LIQUID CRYSTAL DISPLAY AND PANEL THEREFOR

TECHNICAL FIELD

The present invention relates to a liquid crystal display and a panel therefor.

BACKGROUND ART

A typical liquid crystal display ("LCD") includes an upper panel provided with a common electrode and color filters, a lower panel provided with thin film transistors ("TFTs) and pixel electrodes, and a liquid crystal layer is interposed therebetween. The pixel electrodes and the common electrode are applied with different electric voltages to generate electric field, thereby changing the orientations of liquid crystal molecules and thus the transmittance of light passing through the liquid crystal layer. As a result, the LCD displays desired images.

However, the LCD has gray inversion that the luminances between grays are reversed and lateral gamma curve distortion that a lateral gamma curve does not coincide with a front gamma curve, thereby exhibiting inferior visibility at left and right view. For example, the luminance increases and the color moves into white as goes toward the lateral side. In particular, the luminance difference between bright grays disappears such that the image is not clear. In the meantime, the recent employment of the LCD at multimedia increasingly requires good visibility for viewing pictures and moving pictures.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more apparent by describing embodiments thereof in detail with reference to the accompanying drawings in which:

Fig. 1 is a layout view of a TFT array panel for an LCD according to a first embodiment of the present invention;

Fig. 2 is a sectional view of the TFT array panel shown in Fig. 1 taken along the line II-II';

Fig. 3 is an equivalent circuit diagram of an LCD according to the first embodiment of the present invention;

Fig. 4 is a layout view of a TFT array panel for an LCD according to the second embodiment of the present invention;

Fig. 5 is a sectional view of the TFT array panel shown in Fig. 4 taken along the line V-V';

Fig. 6 is an equivalent circuit diagram of an LCD according to the second embodiment of the present invention;

Fig. 7 is a layout view of an LCD according to the third embodiment of the present invention;

Fig. 8 is an equivalent circuit diagram of an LCD according to the third embodiment of the present invention.

Fig. 9 is a layout view of an LCD according to the fourth embodiment of the present invention;

Fig. 10 is an equivalent circuit diagram of an LCD according to the fourth embodiment of the present invention;

Fig. 11 is a layout view of a TFT array panel for an LCD according to the fifth embodiment of the present invention;

Fig. 12 is a layout view of a color filter panel for an LCD according to the fifth embodiment of the present invention;

Fig. 13 is a layout view of an LCD the fifth embodiment of the present invention;

Fig. 14 is a sectional view of the LCD shown in Fig. 13 taken along the line XIV-XIV';

Fig. 15 is an equivalent circuit diagram of an LCD according to the sixth embodiment of the present invention; and

Fig. 16 is an equivalent circuit diagram of an LCD according to the seventh embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

TECHNICAL PROBLEM

A motivation of the present invention is to provide a liquid crystal display having excellent visibility.

TECHNICAL SOLUTION

Based on the motivation, the present invention divides a pixel electrode into two sub-electrodes and applies different voltages to the sub-electrodes.

In detail, a thin film transistor array panel according to an embodiment of the present invention includes a plurality of first signal lines and a plurality of second signal lines insulated from the first signal lines and intersecting the first signal lines formed on the insulating substrate. A plurality of first pixel electrodes are disposed on pixel areas defined by intersections of the first signal lines and the second signal lines and arranged in a matrix and a plurality of first thin film transistors, each having three terminals connected to one of the first signal lines, one of the second signal lines, and one of the first pixel electrodes, are formed thereon. A plurality of second pixel electrodes are disposed on the pixel areas and capacitively coupled to the first pixel electrodes, and a plurality of second thin film transistors are formed thereon. Each of the second thin film transistors have a terminal connected to one of the second pixel electrodes and another terminal connected to one of the first signal lines that is connected to one of the first pixel electrodes in a pixel area in an adjacent row.

The thin film transistor array panel may further include a plurality of coupling electrodes that are connected to or overlapping the first pixel electrodes and overlap the second pixel electrodes with being insulated therefrom. The coupling electrodes are preferably connected to drain electrodes of the first thin film transistors connected to the first pixel electrodes.

The thin film transistor array panel may further include a plurality of third signal lines intersecting the second signal lines, wherein a final terminal of each of the second thin film transistors is connected to one of the third signal lines and the second signal lines.

The final terminal of each of the second thin film transistors may be connected to one of the third signal lines, and the thin film transistor array panel may further include a plurality of third thin film transistors, each having three terminal connected to one of the second signal lines, one of the second pixel electrodes, and one of the first signal lines connected to a pixel area in an adjacent row.

At least one of the first pixel electrodes and the second pixel electrodes includes at least one domain partitioning member. The thin film transistor array panel may further include a gate insulating layer disposed between the first signal lines and the second signal lines, and a passivation layer disposed between the second signal lines and the first and the second pixel electrodes, wherein the coupling electrodes are preferably connected to the first pixel electrodes through contact holes at the passivation layer.

The thin film transistor array panel according to embodiments of the present invention is used for a panel for a liquid crystal display.

ADVANTAGEOUS EFFECT

A viewing angle of an LCD is enlarged by improving lateral visibility.

BEST MODE OF EMBODIMENTS

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the inventions invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

Then, liquid crystal displays and thin film transistor panels therefor according to embodiments of this invention will be described in detail with reference to the accompanying drawings.

Fig. 1 is a layout view of a TFT array panel for an LCD according to a first embodiment of the present invention, Fig. 2 is a sectional view of the TFT array panel shown in Fig. 1 taken along the line II-II', and Fig. 3 is an equivalent circuit diagram of an LCD according to the first embodiment of the present invention.

An LCD according to an embodiment of the present invention includes a lower panel (i.e., a TFT array panel), an upper panel (i.e., an opposite panel) facing the lower panel, and a liquid crystal layer interposed between the two panels and including liquid crystal molecules aligned in a twisted nematic mode such that they are twisted from the lower panel to the upper panel.

First, the lower panel is described.

A plurality of first and second pixel electrodes 190a and 190b preferably made of transparent conductive material such as ITO (indium tin oxide) and IZO (indium zinc oxide) are formed on an insulating substrate 110 preferably made of transparent insulating material such as glass. Each of the first pixel electrodes 190a is connected to a first thin film transistor TFT1 and receives image signal voltages therefrom, and each of the second pixel electrodes 190b is connected to a second thin film transistor TFT2 that is electrically connected to a previous gate line 121 for transmitting gate signals or scanning signals to a previous pixel row and to a storage electrode line 131. The second pixel electrode 190b overlaps a coupling electrode 176 connected to the first pixel electrode 190a to be electromagnetically (capacitively) coupled therewith. The first thin film transistor TFT1 is connected to a gate line 121 transmitting scanning signals and a data line 171 transmitting image voltages and switches on or off the image signals to be supplied to the first pixel electrode 190a in response to the scanning signals. Here, the first and the second pixel electrodes 190a and 190b for a reflective LCD may not include transparent material.

In the meantime, although it is not shown in the figures, the upper panel is described now.

A black matrix for blocking light leakage between pixels, a plurality of red, green, and blue color filters, and a common electrode preferably made of transparent conductive material such as ITO and IZO for generating an electric field along with the pixel electrodes 190a and 190b are formed a surface of an insulating substrate preferably made of transparent insulating material such as glass, which faces the TFT array panel. The black matrix and the color filters may be provided on the TFT array panel.

Now, a TFT array panel for an LCD according to the first embodiment is described more in detail.

A plurality of gate lines 121 and a plurality of storage electrode lines 131 extending in a transverse direction are formed on a lower insulating substrate 110.

A plurality of portions of each gate line 121 expand upward and downward to a plurality of gate electrodes 123a of first thin film transistors TFT1, and each gate lines 121 includes an end portion 125 having a large area for connection with an external circuit.

In the meantime, a gate line 121 transmitting gate signals or scanning signals to a previous pixel row has a plurality of portions forming gate electrodes 123b of second thin film transistors TFT2.

Each pixel electrode 131 includes a plurality of sets of storage electrodes 133a and 133b branched therefrom. Two storage electrodes 133a and 133b in a set of storage electrodes 133a and 133b are branched out in a longitudinal direction and extend to edges of a pixel area.

The gate lines 121 and the storage electrode lines 131 is preferably made of metal such as Al, Al alloy, Ag, Ag alloy, Cr, Ti, Ta and Mo. As shown in Fig. 2, the gate lines 121 and the storage electrode lines 131 according to this embodiment including a single layer. However, they may have a dual-layered structure including a metal layer preferably made of Cr, Mo, Ti and Ta having excellent physical and chemical characteristics and another metal layer preferably containing Al or Ag having low resistivity. The gate lines 121 ad the storage electrode lines 131 may be made of various metal or conductors other than those described above.

The gate lines 121 and the storage electrode lines 131 have inclined side surfaces and the inclination angle relative to a horizontal surface is preferably 30-80°.

A gate insulating layer 140 preferably made of silicon nitride SiNx is formed on the gate lines 121 and the storage electrode lines 131.

On the gate insulating layer 140, a plurality of the data lines 171 을 비롯하여 a plurality of drain electrodes 175 of the first thin film transistors TFT1,

a plurality of coupling electrodes 176, and a plurality of under-bridge metal pieces 172 are formed. Each data line 171 extends substantially in the longitudinal direction, and it includes a plurality of branches extending to the drain electrodes 175 to form source electrodes 173a of the first thin film transistors TFT1. The under-bridge metal pieces 172 are disposed on previous gate lines 121 and include a plurality portions forming drain electrodes 175b of the second thin film transistors TFT2. A plurality of source electrodes 173b of the second thin film transistors TFT2 are formed on the previous gate lines 121 and they are disposed opposite to the drain electrodes 175b of the second thin film transistors TFT2 with respect to the previous gate lines 121. The coupling electrodes 176 are connected to the drain electrodes 175a of the first thin film transistors TFT1 and disposed near the pixel areas to overlap the storage electrode lines 131.

The data lines 171, the drain electrodes 175a and 175b, the coupling electrodes 176, the source electrodes 173a and 173b, and the under-bridge metal pieces 172 are preferably made of Cr or Al like the gate lines 121, and they may include a single layer or multiple layers.

A plurality of semiconductor stripes 151 are formed under the data lines 171 and the drain electrodes 175a and they extend substantially in the longitudinal direction along the data lines 171. Each semiconductor stripe 151 preferably made of amorphous silicon has a plurality of branches extending toward the gate lines 123a, the source electrodes 173a, and the drain electrodes 175a and forming channel portions 154 of the first thin film transistors TFT1. In addition, a plurality of semiconductor islands 155 forming channel portions of the second thin film transistors TFT2 are formed on the previous gate lines 121.

A plurality of ohmic contacts 161 are disposed between the semiconductors 151 and the data lines 171 and the drain electrodes 175a for reducing the contact resistance therebetween. The ohmic contacts 161 are preferably made of silicide or amorphous silicon heavily doped with n type impurity. The ohmic contacts 161 include a plurality of ohmic contacts 163a and 165a for the first thin film transistors TFT1 disposed under the source electrodes 173a and the drain electrodes 175a, and a plurality of ohmic contacts 163b and

165b for the second thin film transistors TFT2 are formed under the source electrodes 173b and the drain electrodes 175b of the second thin film transistors TFT2.

A passivation layer 180 made of an inorganic insulator such as silicon nitride or an organic insulator such as resin is formed on the data lines 171, the drain electrodes 175a and 175b, the coupling electrodes 176, and the under-bridge metal pieces 172.

The passivation layer 180 has a plurality of contact holes 181a, 181b and 183 exposing at least a portion of the drain electrodes 175a and 175b and the end portions 179 of the data lines 171, respectively. In addition, a plurality of contact holes 182, 184 and 185 exposing the end portions 125 of the gate lines 121 and portions of the storage electrode lines 131, respectively, penetrate the gate insulating layer 140 and the passivation layer 180. In addition, the passivation layer 180 has a plurality of contact holes 186 exposing the source electrodes of the second thin film transistors TFT2.

A plurality of pixel electrodes the pixel electrodes 190a and 190b, a plurality of contact assistants 95 and 97, and a plurality of storage bridges 91 are formed on the passivation layer 180. The pixel electrodes 190a and 190b, the contact assistants 95 and 97, and the storage bridges 91 is preferably made of a transparent conductor such as ITO (indium tin oxide) and IZO (indium zinc oxide) or an opaque conductor such as Al having excellent light reflectance.

The pixel electrodes 190a and 190b includes first pixel electrodes 190a and second pixel electrodes 190b. The first pixel electrodes 190a are connected to the drain electrodes 175a of the first thin film transistors TFT1 through the contact holes 181a, and the second pixel electrodes 190b are connected to the drain electrodes 175b of the second thin film transistors TFT2 through the contact holes 181b and overlap the coupling electrodes 176. Accordingly, the second pixel electrodes 190b are electromagnetically (capacitively) coupled to the first pixel electrodes 190a.

The storage bridges 91 connect two storage electrode lines 131 disposed opposite each other with respect to the gate lines 121. The storage bridges 91 contact the storage electrodes 133a and the storage electrode lines 131 through

the contact holes 184 and 185 penetrating the passivation layer 180 and the gate insulating layer 140. The storage bridges 91 are connected to the under-bridge metal pieces 172 through the contact holes 186. Accordingly, when the second thin film transistors operate responsive to gate-on signals applied to the previous gate lines 121, the second pixel electrodes 190b are supplied with a common voltage or a reference voltage applied to the storage electrode lines 131. The storage bridges 91 electrically connect all the storage electrode lines 131 on the lower substrate 110. The storage electrode lines 131 are used for repairing the defects in the gate lines 121 or the data lines 171, if necessary, and the under-bridge metal pieces 172 enhance the electrical connection between the gate lines 121 and the storage bridges 91 when a laser beam is illuminated for repairing.

The contact assistants 95 and 97 are connected to the end portions 125 of the gate lines 121 and the end portions 179 of the data lines 171 through the contact holes 182 and 183, respectively.

In the above-described LCD, the first pixel electrodes 190a receive the image signal voltages through the first thin film transistors TFT1, while the second pixel electrodes 190b have changing voltages dependent on the capacitive coupling with the storage electrode lines 131. Therefore, absolute values of the voltages of the second pixel electrodes 190b are always higher than those of the first pixel electrodes 190a. In this way, two pixel electrodes disposed in a pixel area but having different voltages compensate their voltages to reduce the distortion of a gamma curve.

Then, a reason why the voltage of a second pixel electrode 190b is maintained higher than that of a first pixel electrode 190a is described with reference to Fig. 3.

In Fig. 3, C_{LCA} indicates a liquid crystal capacitance between a first pixel electrode 190a and a common electrode of an opposite panel, and C_{STA} indicates a storage capacitance between the first pixel electrode 190a and a storage electrode line 131. C_{LCB} indicates a liquid crystal capacitance between a second pixel electrode 190b and the common electrode of the opposite panel, C_{STB} indicates a storage capacitance between the second pixel electrode 190b and the storage

electrode line 131, and C_{CPB} indicates a coupling capacitance between a coupling electrode 176 and the second pixel electrode 190b.

The voltage of the first pixel electrode 190a with respect to a common voltage or a reference voltage applied to the common electrode of the opposite panel is denoted by Va(Vd1), and the voltage of the second pixel electrode 190b is denoted by Vb. The voltage distribution law results in:

$$Vb \approx 1/(C_1+2C_2)\times[(2-C_3/C_2)\times(C_1+C_2)\times Vd1].$$

The voltage Vb can be controlled such that the voltage Vb approaches the voltage Va but always higher than the voltage Va by adjusting the capacitances. Here, $C_1=C_{LCA}+C_{STA}$, $C_2=C_{CPB}$, and $C_3=C_{LCB}+C_{STB}$. A parasitic capacitance between a gate electrode and a source electrode is neglected since it is trivial.

The arrangements of the first or the second thin film transistor TFT1 or TFT2 or the connection between the first and the second pixel electrodes 190a and 190b can be variously modified, which will be described in second to seventh embodiments.

Hereinafter, only the features distinguished from the first embodiment will be described and remaining features that is the same as those of the first embodiment will be omitted.

Fig. 4 is a layout view of a TFT array panel for an LCD according to the second embodiment of the present invention, Fig. 5 is a sectional view of the TFT array panel shown in Fig. 4 taken along the line V-V', and Fig. 6 is an equivalent circuit diagram of an LCD according to the second embodiment of the present invention.

In the TFT array panel for an LCD according to the second embodiment, a second thin film transistor TFT2 is driven though a previous gate line 121 like the first embodiment, but it owns a gate electrode 123 commonly with a first thin film transistor TFT1 and the first and the second thin film transistors TFT1 and TFT2 are disposed opposite with respect to a gate line 121. A source electrode 173b of the second thin film transistor TFT2 and a source electrode 173a of the first thin film transistor TFT1 extend from a data line 171, a drain electrode 175b

of the second thin film transistor TFT2 extends opposite a drain electrode 175a of the first thin film transistor TFT1 with respect to the gate electrode 123.

In the TFT array panel for an LCD according to the second embodiment of the present invention, although a second pixel electrode 190b is initially supplied with a pixel voltage supplied with a first pixel electrode 190a of a previous pixel row, it is supplied with a voltage Vb close to a voltage Va(Vd1) of the first pixel electrode 190a when the pixels in a corresponding pixel row are driven since it is capacitively coupled with the first pixel electrode 190a. The voltage Vb is given from the voltage distribution law by:

$$Vb \approx 1/(C_1+2C_2)\times[(2-C_3/C_2)\times(C_1+C_2)\times Vd1+(C_1+C_3)Vd2].$$

The voltage Vb can be controlled such that the voltage Vb approaches the voltage Va but always higher than the voltage Va by adjusting the capacitances and the TFT array panel according to the second embodiment of the present invention is preferably subject to column inversion therefor. Here, the voltage Vd2 is the voltage initially supplied to the second pixel electrode 190b when the second thin film transistor TFT2 turns on.

The first and the second embodiments according to the present invention the second relates to the control of an effective driving voltage supplied to the pixel electrode 190b. However, the TFT array panel may be modified such that the first pixel electrode 190a is supplied with a voltage lower than a driving voltage transmitted by a data line, while the second pixel electrode 190b is supplied with a voltage higher than the driving voltage, which will be described in detail with reference to the figures.

Fig. 7 is a layout view of an LCD according to the third embodiment of the present invention and Fig. 8 is an equivalent circuit diagram of an LCD according to the third embodiment of the present invention.

Most of the configuration is the same as those shown in Figs. 1 and 3.

However, a first pixel electrode 190a is not connected to a first thin film transistor TFT1 through a contact hole in a passivation layer (indicated by 180 in Fig. 2), and it overlaps a coupling electrode 176 such that it is electromagnetically (capacitively) coupled with the first thin film transistors TFT1.

In the TFT array panel for an LCD according to the third embodiment of the present invention, an effective pixel voltage supplied to a first pixel electrode 190a is smaller than a voltage Vd1 supplied through a data line 171. It is because that the first pixel electrode 190a is capacitively coupled with the coupling electrodes 176 connected to a drain electrode 175a, the effective pixel voltage Va of the first pixel electrode 190a with respect to the common voltage is given from the voltage distribution law by:

$$Va=Vd1\times[C_{CPA}/(C_{CPA}+C_{LCB})].$$

Since $C_{CPA}/(C_{CPA}+C_{LCB})$ is always lower than one, the voltage Va is always smaller than the voltage Vd1. Here, C_{CPA} indicates a coupling capacitance between the coupling electrodes 176 and the first pixel electrode 190a.

The effective driving voltage Vb supplied to the second pixel electrode 190b is determined in the same way as the first embodiment.

Fig. 9 is a layout view of an LCD according to the fourth embodiment of the present invention and Fig. 10 is an equivalent circuit diagram of an LCD according to the fourth embodiment of the present invention.

Most of the configuration is the same as those shown in Figs. 4 and 6.

However, the connection relation between first and second thin film transistors TFT1 and TFT2 and the first and the second pixel electrodes 190a and 190b is substantially the same as that shown in Figs. 7 and 8.

In this case, an effective driving voltage Vb supplied to the first pixel electrode 190a is smaller than a voltage Vd1 transmitted by a data line 171 and an effective driving voltage Vb supplied to the second pixel electrode 190b is determined in the same way as the second embodiment.

The LCD has a major disadvantage of its narrow viewing angle, and several suggestions increasing the viewing angle for overcoming the disadvantage have been developed. Among these techniques, a method provides a plurality of cutouts or a plurality of protrusions on pixel electrodes and a common electrode opposite each other and aligns liquid crystal molecules vertical to upper and lower panels. The cutouts or the protrusions can be applied to TFT array panels according to embodiments of the present invention.

The cutouts provided both at the pixel electrodes and the common electrode give wide viewing angle by generating fringe field to adjust the tilt directions of the liquid crystal molecules.

The provision of the protrusions both on the pixel electrode and the common electrode in the lower and upper panels distorts the electric field to adjust the tilt directions of the liquid crystal molecules.

The fringe field for adjusting the tilt directions of the liquid crystal molecules to form a plurality of domains is also obtained by providing the cutouts at the pixel electrodes on the lower panel and the protrusions on the common electrode on the upper panel.

The fifth embodiment of the present invention relates to a configuration having cutouts is described in detail.

Fig. 11 is a layout view of a TFT array panel for an LCD according to the fifth embodiment of the present invention, Fig. 12 is a layout view of a color filter panel for an LCD according to the fifth embodiment of the present invention, Fig. 13 is a layout view of an LCD the fifth embodiment of the present invention, and Fig. 14 is a sectional view of the LCD shown in Fig. 13 taken along the line XIV-XIV'.

An LCD according to the fifth embodiment of the present invention includes a lower panel, an upper panel facing the lower panel, and a liquid crystal layer interposed between the two panels and including liquid crystal molecules aligned vertical to surfaces of the panels.

First, the lower panel is described.

A plurality of first and second pixel electrodes 190a and 190b preferably made of transparent conductive material such as ITO (indium tin oxide) and IZO (indium zinc oxide) are formed on an insulating substrate 110 preferably made of transparent insulating material such as glass. The first and the second pixel electrodes 190a and 190b are connected to first and second thin film transistors TFT1 and TFT2, respectively, like the first embodiment. Each of the second pixel electrodes 190b overlaps a coupling electrode 176 connected to a first pixel electrode 190a to be electromagnetically (capacitively) coupled therewith. The second pixel electrode 190b has a cutout 192. A lower polarizing plate 12 is

attached to an outer surface of the insulating substrate 110. Here, the first and the second pixel electrodes 190a and 190b for a reflective LCD may not include transparent material, and in this case, the lower polarizing plate 12 is unnecessary.

The upper panel is described now.

A black matrix 220 for blocking light leakage between pixels, a plurality of red, green, and blue color filters 230, and a common electrode 270 preferably made of transparent conductive material such as ITO and IZO are formed on an inner surface of an insulating substrate 210 preferably made of transparent insulating material such as glass. The common electrode 270 has a plurality of cutouts 271, 272 and 273. The black matrix 220 is disposed around pixel areas and it may overlap the cutouts 271, 272 and 273 of the common electrode 270 for blocking light leakage near edges of the cutouts 271, 272 and 273.

Now, a TFT array panel for an LCD according to the first embodiment is described more in detail.

A pair of a first pixel electrode 190a and a second pixel electrode 190b is divided by a gap that includes a pair of portions 191 and 193 making 45 degrees with gate line 121 and a portion perpendicular to the gate lines 121. Each of the 45-degree portions 191 and 193 is longer than the perpendicular portion. In addition, the 45-degree portions are perpendicular to each other.

A second pixel electrode 190b has a cutout 192 that extends from a right edge of the second pixel electrode 190b toward a left edge thereof and has an expanded inlet.

The first pixel electrode 190a and the second pixel electrode 190b have inversion symmetry with respect to a line that bisects a pixel area defined by intersections of the gate lines 121 and data lines 171 (and extends parallel to the gate lines 121).

A black matrix 220 for blocking light leakage is formed on an upper insulating substrate 210 and a plurality of red, green, and blue color filters 230 are formed on the black matrix 220. A common electrode 270, which is preferably made of transparent conductive material such as ITO and IZO and includes a plurality of sets of cutouts 271-273 are formed on the color filters 230.

A set of the cutouts 271, 272 and 273 in the common electrode 270 interpose the 45-degree portions of the gap between the pixel electrodes 190a and 190b and they include oblique portions parallel to the 45-dgree portions and end portions overlapping edges of the pixel electrodes 190a and 190b. The end portions of the cutouts 271-273 include longitudinal end portions and transverse end portions.

The above-described TFT array panel and color filter panel are aligned and assembled and a liquid crystal material is injected therebetween and vertically aligned, thereby preparing a basic structure of the LCD according to an embodiment of the present.

When the TFT array panel and the color filter panel are aligned with each other, a set of the cutouts 271, 272 and 273 in the common electrode 270 partition each of the pixel electrodes 190a and 190b into a plurality of subareas, according to this embodiment, four subareas as shown in Fig. 13. As shown in Fig. 13, each subarea is elongated to have a width direction and a length direction.

Portions of a liquid crystal layer 3 disposed between the subareas of the pixel electrodes 190a and 190b and the subareas of the common electrode 270 corresponding thereto are referred to as subregions, and the subregions are classified into four kinds depending on average long-axis directions of liquid crystal molecules contained therein under the application of an electric field, which are referred to as domains.

In the meantime, although the first to the fifth embodiments connect a second pixel electrode 190b to a second thin film transistor TFT2, the second pixel electrode 190b may be connected to two thin film transistors.

Fig. 15 is an equivalent circuit diagram of an LCD according to the sixth embodiment of the present invention.

Referring to Fig. 15, an LCD according to the sixth embodiment of the present invention adds the second thin film transistor (TFT2 shown in Fig. 6) of the second embodiment into the connection configuration of the first embodiment as a third thin film transistor TFT3.

Fig. 16 is an equivalent circuit diagram of an LCD according to the seventh embodiment of the present invention.

Referring to Fig. 16, an LCD according to the sixth embodiment of the present invention adds the second thin film transistor (TFT2 shown in Fig. 10) of the fourth embodiment into the connection configuration of the third embodiment as a third thin film transistor TFT3.

The above-described configuration improves lateral visibility of an LCD, thereby widening a viewing angle.

While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims. In particular, the cutouts formed in the pixel electrodes and the common electrode have various modifications.